Design Review Checklist

Schematic Circuit Diagram

Last updated: 1/4/2020

- [ ] Ensure that there are no missing net ties and schematic ports across all schematic sheets.

- [ ] Ensure that design rules matching the PCB manufacturer's capabilities have been implemented.

- [ ] Ensure that all component decoupling capacitors be clearly identified, with a proper note about placement close to the supply pins of the processor.

- [ ] Add appropriate notes regarding:

    a. trace width for high current traces

    b. trace length matching for high-speed traces with matching propagation delay requirements.

    c. controlled impedance traces, include the expected impedance of such traces.

    d. traces carrying low noise signals. Indicate that they are to be separated from high current traces or traces carrying fast signals.

    e. trace separation clearances for high voltage trace. Indicate if physical barriers such as PCB slots are needed.

- [ ] Properly identify passive components with specific characteristics such as high power or precision resistors, low temperature coefficient, or low ESR capacitors and others

- [ ] Unused pins on IC's should be confirmed to be no net connection, or pulled up or pulled down.

- [ ] Check all schematic capture compilation warnings. Do not ignore any unless there is a good reason for doing so.

- [ ] Ensure the IC outputs such as I2C SDA or SCL have proper pull-up resistors.

- [ ] Ensure that clamp diodes and transient suppressors have been included in all externally exposed connections.

- [ ] If there are different types of Ground, eg. Signal ground or Power ground, make sure to properly label each ground with its type.

- [ ] Identify magnetic components, such as power inductors, that could cross-couple. Make a note about properly spacing, or orienting, them.

- [ ] Identify high heat generating components and temperature sensitive components, and add a note that they are to be properly physically separated.

- [ ] Identify circuit sections that need to be shielded, and indicate the type of shielding, such as cans, needed.

- [ ] Indicate the need of guard rings around very sensitive low-level signal input pins.

- [ ] Do not place high voltage and low voltage lines adjacent to each other on connector pins on the schematic.

- [ ] Use multiple connector pins for carrying high current, taking into account the current carrying capability of each pin of the selected connector.

- [ ] If using PCB heatsink or on-board heatsinks, specify keep-out area.

- [ ] Specify Do-Not-Populate (DNP) components.

- [ ] Add appropriate test points to critical nodes.

- [ ] Specify test point surface treatment, if required.

- [ ] Specify surface treatment, such as gold plating of a given thickness, for edge connector fingers.