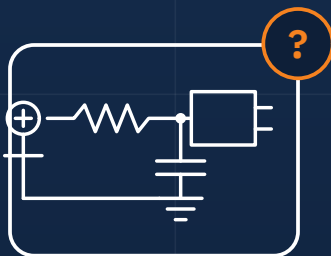


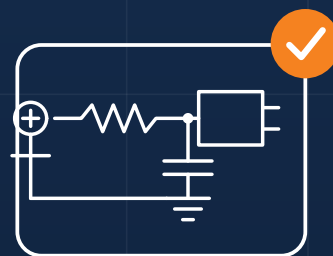
REVIEW THE SCHEMATIC BEFORE LAYOUT STARTS

SCHEMATIC DESIGN REVIEW CHECKLIST

60 checks covering the schematic, component selection, and bill of materials. Work through them before layout is released.



DESIGN FILES
UNVERIFIED



RELEASE PACKAGE
MANUFACTURING READY

PREPARED BY
JOHN TEEL

DOC NO.
MRR-01

REV
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SOURCE
PREDICTABLEDESIGNS.COM

Schematic Design Review Checklist

Manufacturing readiness review of the schematic, component selection, and bill of materials.

This checklist covers the schematic, the parts chosen for it, and the bill of materials in a single pass. Work through it once the schematic is considered complete and before layout is released, because every item on it is cheaper to fix now than after boards are built. Before starting, ask the design owner for the schematic, the BOM, and a distributor BOM report (a Digi-Key, Mouser, or Octopart upload).

How to use this checklist

Click a box to check off an item once it has been verified against the design. Type comments, waivers, or follow-ups in the Notes field beside it. Sections marked IF APPLICABLE can be skipped for designs that do not use them. Record the overall result in the Review Summary at the end.

Review Information

PRODUCT / PROJECT

DESIGN REVISION

DESIGN OWNER

REVIEWER

REVIEW DATE

REVIEW TYPE

The Checklist at a Glance

#	SECTION	APPLIES TO	CHECKS
1	Components & BOM	Every design	10
2	Power, Protection & EMC	Every design	10
3	Bypass & Decoupling	Every design	4
4	Clock & Timing	Every design	3
5	Digital Interfaces	Every design	8
6	Analog Circuits	Every design	8
7	IC Pin Configuration	Every design	3
8	RF & Wireless	If applicable	4
9	Programming, Test & Debug	Every design	4
10	Documentation & ERC	Every design	6

60 checks across 10 sections. Sections marked "if applicable" only count when the design uses that feature or process.

#1	Components & BOM	10 CHECKS
CHECK	NOTES	
☐ Every part has a manufacturer part number (MPN) assigned, and DNP (do-not-populate) parts are clearly marked		
☐ Non-schematic parts (standoffs, screws, labels, gaskets, cables) are added to the BOM		
☐ MPN package variant matches the schematic symbol and footprint for ICs, modules, and connectors (correct package, pin count, and pitch)		
☐ Design owner has supplied a distributor BOM report (Digi-Key, Mouser, or Octopart upload); reviewer has skimmed it for NRND/EOL, out-of-stock, long-lead, and RoHS/REACH flags on ICs, modules, and connectors		
☐ Design owner has identified alternates for single-source critical parts		
☐ BOM cost at production volume confirmed against target by the design owner		
☐ Voltage, current, and power ratings have adequate derating margin (capacitors typically 2x rated voltage, resistors 50% rated power)		
☐ Capacitor effective capacitance verified under DC bias (especially small-package X5R/X7R)		

#1

Components & BOM (continued)

10 CHECKS

CHECK	NOTES
☐ Package types appropriate for assembly (SMT preferred, no unnecessarily small packages), and tall parts flagged for the enclosure check	
☐ BOM revision matches the schematic and layout revision, and approved alternates are documented	

#2

Power, Protection & EMC

10 CHECKS

CHECK	NOTES
☐ Input protection present (reverse polarity, overvoltage)	
☐ Inrush current limiting present if needed	
☐ Supply voltages appropriate for the circuitry, and linear regulator input/output differential within spec (dropout and dissipation)	
☐ Switching regulator has input and output capacitors per the datasheet	
☐ ESD protection (TVS or clamp diodes) on all external-facing connections	
☐ Fuses or PTC devices sized appropriately if present	

#2	Power, Protection & EMC (continued)	10 CHECKS
CHECK	NOTES	
☐ EMC filtering on the power input and external-facing I/O (ferrite beads, common-mode chokes, LC filters)		
☐ Battery protection present if applicable (overcharge, deep discharge, over-current, thermal)		
☐ Brown-out detection, voltage supervisor, or power-on reset present		
☐ Safety-critical isolation maintained where required		

#3	Bypass & Decoupling	4 CHECKS
CHECK	NOTES	
☐ Every IC has at least one decoupling capacitor per power pin		
☐ Decoupling capacitor values match datasheet recommendations for major ICs (MCU, wireless module, PMIC, PHY, high-speed parts)		
☐ Mix of capacitor values present (bulk plus ceramic) where appropriate		
☐ Analog ICs have separate decoupling from digital where recommended		

#4 Clock & Timing		3 CHECKS
CHECK	NOTES	
☐ Crystal load capacitors correct per the datasheet ($CL = C1 \times C2 / (C1 + C2) + C_{stray}$)		
☐ Oscillator circuit matches the datasheet reference design		
☐ Clock distribution buffers present if needed for fanout		

#5 Digital Interfaces		8 CHECKS
CHECK	NOTES	
☐ I2C buses have pullups sized for bus speed and capacitance (typically 2.2k to 10k ohm)		
☐ SPI signals connected correctly (MISO/MOSI not swapped), with chip selects active-low and pulled up where needed		
☐ UART connections correct (TX to RX, RX to TX)		
☐ USB data lines have correct series termination (22 ohm) and D+ pullup (1.5k ohm for full-speed) unless integrated in the controller		
☐ Ethernet has magnetics and correct termination resistors		

#5	Digital Interfaces (continued)	8 CHECKS
CHECK	NOTES	
☐ CAN bus has 120 ohm termination at both ends only		
☐ Level shifters present where signals cross voltage domains		
☐ Logic levels compatible between connected ICs		

#6	Analog Circuits	8 CHECKS
CHECK	NOTES	
☐ Op-amp feedback networks appear reasonable (gain, stability)		
☐ ADC reference voltage is stable (buffered, filtered)		
☐ ADC input range matches expected signal levels		
☐ Input protection present on ADC inputs (clamp diodes, series resistance)		
☐ Anti-aliasing filters present before ADC inputs where needed		

#6	Analog Circuits (continued)	8 CHECKS
CHECK	NOTES	
☐ DAC output has an appropriate load or buffer		
☐ Sensor signal conditioning appears appropriate		
☐ Analog ground separate from digital if used		

#7	IC Pin Configuration	3 CHECKS
CHECK	NOTES	
☐ Configuration, strapping, mode, and enable pins set per the datasheet for major ICs (not left floating)		
☐ Unused inputs have pullups or pulldowns (not left floating)		
☐ Reset pins have pullups if active-low		

#8	RF & Wireless	IF APPLICABLE
CHECK	NOTES	
☐ Antenna connection appropriate (connector or chip antenna) with a 50 ohm matching network		
☐ Balun and matching network match the reference design, with PI network footprints included even if unpopulated		
☐ RF section has appropriate filtering		
☐ Certified wireless module used where appropriate (vs. a bare-chip RF design)		

#9	Programming, Test & Debug	4 CHECKS
CHECK	NOTES	
☐ Programming header present and pinned per the standard (JTAG, SWD, ISP)		
☐ Serial debug port accessible (UART or USB)		
☐ Test points or headers on critical signals		
☐ LED indicators present for power and status		

#10 Documentation & ERC		6 CHECKS
CHECK	NOTES	
☐ ERC run and clean, with any waivers documented		
☐ Component values clearly labeled and readable		
☐ Net names meaningful, and power nets labeled with voltages (3V3, 5V0)		
☐ All IC pins connected or explicitly marked NC (no connect)		
☐ Connector pin numbering is clear		
☐ Schematic organized logically by function		



Review Summary

SIGN-OFF

OVERALL RESULT

☐ Approved for manufacturing ☐ Approved with changes noted ☐ Not approved, re-review required

SUMMARY AND REQUIRED CHANGES

REVIEWER SIGN-OFF

SIGN-OFF DATE