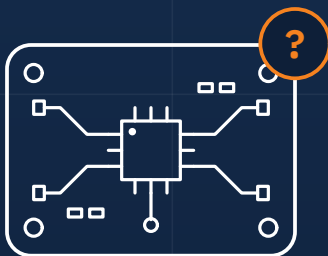


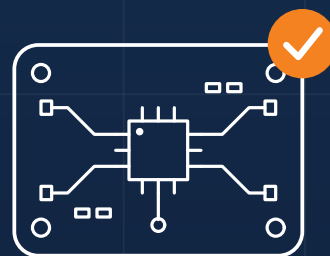
REVIEW THE LAYOUT BEFORE GERBERS GO OUT

PCB LAYOUT DESIGN REVIEW CHECKLIST

65 checks covering placement, routing, power, EMI, thermal, and manufacturability. Work through them before Gerbers go to the fab.



DESIGN FILES
UNVERIFIED



RELEASE PACKAGE
MANUFACTURING READY

PREPARED BY
JOHN TEEL

DOC NO.
MRR-02

REV
B

SOURCE
PREDICTABLEDESIGNS.COM

PCB Layout Design Review Checklist

Manufacturing readiness review of the printed circuit board layout.

This checklist covers the PCB layout before Gerbers are released to the fabricator and assembler. It assumes the schematic has already passed its own review, so it focuses on placement, routing, power, EMI, thermal, and manufacturability rather than circuit design. Before starting, ask the design owner for the layout files, the fab's design rules, and a DRC report run against them.

How to use this checklist

Click a box to check off an item once it has been verified against the design. Type comments, waivers, or follow-ups in the Notes field beside it. Sections marked IF APPLICABLE can be skipped for designs that do not use them. Record the overall result in the Review Summary at the end.

Review Information

PRODUCT / PROJECT

DESIGN REVISION

DESIGN OWNER

REVIEWER

REVIEW DATE

REVIEW TYPE

The Checklist at a Glance

#	SECTION	APPLIES TO	CHECKS
1	Board Structure & Outline	Every design	4
2	Component Placement	Every design	6
3	Power Distribution & Grounding	Every design	9
4	Switching Power Supply Layout	Every design	3
5	High-Speed & Critical Signals	Every design	5
6	RF Layout	If applicable	7
7	Analog Signal Routing	Every design	5
8	Thermal Management	Every design	3
9	Crystal & Oscillator Layout	Every design	2
10	Manufacturing & Assembly	Every design	11
11	Silkscreen & Markings	Every design	4
12	Layer Stackup	Every design	3
13	High Voltage & Safety	If applicable	3

65 checks across 13 sections. Sections marked "if applicable" only count when the design uses that feature or process.

#1	Board Structure & Outline	4 CHECKS
CHECK	NOTES	
☐ Board dimensions and outline match the mechanical and enclosure requirements		
☐ Mounting holes present and properly sized, with keepouts for screw heads and standoffs		
☐ Corner radius appropriate for manufacturability		
☐ PCB thickness specified in the stackup		

#2	Component Placement	6 CHECKS
CHECK	NOTES	
☐ Components grouped logically by function		
☐ High-power components not clustered, and temperature-sensitive components placed away from heat sources		
☐ Tall components positioned to avoid mechanical interference		
☐ Connectors accessible (not blocked by other components) and mechanically reinforced where needed (mounting tabs, brackets)		

#2	Component Placement (continued)	6 CHECKS
CHECK	NOTES	
☐ Components with thermal pads positioned for heat management		
☐ Adequate spacing between components for assembly, with no components too close to the board edge		

#3 Power Distribution & Grounding		9 CHECKS
CHECK	NOTES	
☐ Power traces and connector pins sized for the expected current		
☐ Multiple vias used on high-current connections		
☐ Decoupling capacitors placed immediately adjacent to IC power pins		
☐ Bulk capacitors positioned near the power input		
☐ Ground plane present and continuous		
☐ Power planes used appropriately, with no long thin power traces creating bottlenecks		

#3	Power Distribution & Grounding (continued)	9 CHECKS
CHECK	NOTES	
☐ Star-point grounding implemented if the design uses a split ground		
☐ Ground stitching vias around the board perimeter and near RF and high-speed sections		
☐ Traces not routed along board edges		

#4	Switching Power Supply Layout	3 CHECKS
CHECK	NOTES	
☐ Hot loop area minimized (input capacitor, switch, and diode or synchronous FET kept tight)		
☐ Feedback trace routed away from the switching node		
☐ Full compare against the manufacturer's reference layout for switchers above about 1 A, or whenever the hot-loop check looks off		

#5	High-Speed & Critical Signals	5 CHECKS
CHECK	NOTES	
☐ Differential pairs routed together with consistent spacing and matched lengths		
☐ High-speed signals have a continuous ground reference beneath (no plane splits crossed)		
☐ Clock signals short and direct, with no stubs and not run parallel to other signals		
☐ Via count minimized on critical signals		
☐ Controlled-impedance traces have the correct width for the stackup		

#6	RF Layout	IF APPLICABLE
CHECK	NOTES	
☐ RF traces are 50 ohm controlled impedance with a ground plane beneath		
☐ Antenna keepout maintained per the antenna datasheet (no copper beneath or beside it)		
☐ Ground stitching vias around the RF section		

#6	RF Layout (continued)	IF APPLICABLE
CHECK	NOTES	
☐ RF traces kept away from digital signals		
☐ Matching network layout matches the reference design, with PI network footprints placed for antenna tuning		
☐ U.FL connector or coax test pad present for RF testing		
☐ RF supply rail filtering present (separate from general decoupling)		

#7	Analog Signal Routing	5 CHECKS
CHECK	NOTES	
☐ Analog traces routed away from digital and switching signals		
☐ Analog ground separate or star-connected if used		
☐ ADC input traces kept short and direct		
☐ Guard rings around sensitive analog inputs if needed		
☐ Differential analog signals routed as pairs		

#8	Thermal Management	3 CHECKS
CHECK	NOTES	
☐ Thermal vias under power components, with adequate count (typically 9 or more) and not tented		
☐ Copper area around hot components for heat spreading		
☐ Heatsink mounting provisions present if needed		

#9	Crystal & Oscillator Layout	2 CHECKS
CHECK	NOTES	
☐ Crystal, load capacitors, and traces placed close to the IC, with short traces and no vias		
☐ Solid ground plane under the crystal, kept away from board edges, connectors, and high-speed signals		

#10	Manufacturing & Assembly	11 CHECKS
CHECK	NOTES	
☐ Design owner has supplied a DRC report run against the fab's design rules, and it is clean or waivers are documented		
☐ 3D view pass: every component's 3D body sits on its pads with no obvious size or orientation mismatch		
☐ Land patterns verified against the datasheet for high-risk packages only: connectors, modules, QFN/DFN and other thermal-pad parts, BGA and fine-pitch (0.5 mm or under) parts, and crystals		
☐ Pin 1 orientation on every IC footprint matches the schematic symbol and datasheet		
☐ Fiducials present (minimum 3, asymmetric, unobscured), with local fiducials near fine-pitch parts		
☐ Component orientation consistent where possible, and fine-pitch parts oriented for easier inspection		

#10
Manufacturing & Assembly (continued)
11 CHECKS

CHECK	NOTES
☐ Via-in-pad filled and capped if used	
☐ Thermal reliefs on plane connections for through-hole and hand-soldered parts	
☐ Cable strain relief provisions present where needed	
☐ Assembly notes flag hand-soldered, orientation-sensitive, and temperature-sensitive parts	
☐ Test points and programming header accessible, with test-fixture requirements noted	

#11	Silkscreen & Markings	4 CHECKS
CHECK	NOTES	
☐ All ICs have pin 1 clearly marked		
☐ Polarized components have polarity marked (+/-, cathode stripe)		
☐ Reference designators present and readable, with silkscreen not covering pads or vias		
☐ Board part number and revision visible on the silkscreen		

#12	Layer Stackup	3 CHECKS
CHECK	NOTES	
☐ Ground layers positioned adjacent to signal layers for return paths		
☐ Controlled-impedance requirements specified to the manufacturer		
☐ Fab's standard stackup used, or symmetry and layer thicknesses reviewed if custom		

#13

High Voltage & Safety

IF APPLICABLE

CHECK

NOTES

☐

Creepage and clearance distances meet the applicable safety standard

☐

Copper removed under isolation areas, with no routing across isolation boundaries

☐

Conformal coating areas defined if applicable



Review Summary

SIGN-OFF

OVERALL RESULT

☐

Approved for manufacturing

☐

Approved with changes noted

☐

Not approved, re-review required

SUMMARY AND REQUIRED CHANGES

REVIEWER SIGN-OFF

SIGN-OFF DATE